CLAIMS

1. An AM intermediate frequency variable gain amplifier circuit, comprising:

first and second field-effect transistors for differentially amplifying an input signal and an inverted input signal obtained by inverting the input signal;

a third field-effect transistor that is connected between a source of the first field-effect transistor and a source of the second field-effect transistor and to the gate of which a control voltage for controlling differential amplification gain of the first and second field-effect transistors; and

a bias circuit for applying a DC bias voltage for operating the third field-effect transistor in a non-saturated region.

2. The AM intermediate frequency variable gain amplifier circuit according to claim 1, wherein

the bias circuit comprises at least a fourth field-effect transistor comprising a source connected to a power supply and a gate and drain connected together.

3. The AM intermediate frequency variable gain amplifier circuit according to claim 1, wherein

the bias circuit comprises at least a fourth field-effect transistor comprising a source connected to a power source and a gate and drain connected together, and a fifth field-effect transistor that is connected to the fourth field-effect transistor in series comprising a gate and drain connected together.

4. The AM intermediate frequency variable gain amplifier circuit according to claim 1, 2 or 3, wherein

a resistor is connected in parallel with the third field-effect transistor.

5. A variable gain amplifier circuit, comprising:

first and second field-effect transistors for differentially amplifying an input signal and an inverted input signal obtained by inverting the input signal;

a third field-effect transistor which is connected between a source of the first field-effect transistors and a source of the second field-effect transistor and to a gate of which a control voltage for controlling differential amplification gain of the first and second field-effect transistors is applied; and

a bias circuit comprising at least a fourth field-effect transistor comprising a source connected to a power supply and a gate and drain connected together, and

which supplies a DC bias voltage for operating the third field-effect transistor in a non-saturated region.

6. The variable gain amplifier circuit according to claim 5, wherein

the bias circuit comprises a fifth field-effect transistor that is connected to the fourth field-effect transistor in series comprising a gate and drain connected together.

7. The variable gain amplifier circuit according to claim 5, comprising

a constant current circuit for supplying constant current to the sources of the first and second MOS transistors.

8. A variable gain amplifier circuit, comprising:

first and second field-effect transistors for differentially amplifying an input signal and a signal obtained by inverting the input signal;

a third field-effect transistor that is connected between a source of the first field-effect transistor and a source of the second field-effect transistor and a control voltage for controlling differential amplification gain of the first and second field-effect transistors is applied

to a gate of the third field-effect transistor;

a first bias circuit which comprises at least a fourth field-effect transistor comprising a source connected to a power supply and a gate and drain connected together and supplies a DC bias voltage for operating the third field-effect transistor in a non-saturated region; and

a second bias circuit which comprises a fifth field-effect transistor comprising source connected to a power supply and a gate and drain connected together and supplies the first and second field-effect transistors with a DC bias voltage.

9. A semiconductor integrated circuit on the semiconductor circuit board of which is formed a variable gain amplifier circuit by a CMOS process, comprising:

first and second MOS transistors for differentially amplifying an input signal and a signal obtained by inverting the input signal;

a third MOS transistor that is connected between a source of the first MOS transistor and a source of the second MOS transistor and a control voltage for controlling differential amplification gain of the first and second MOS transistors is applied to a gate of the third MOS transistor; and-

a bias circuit which comprises a fourth MOS transistor

comprising a source connected to a power supply and a gate and drain is connected together and supplies a DC bias voltage for operating the third MOS transistor in a non-saturated region.

10. A semiconductor integrated circuit on the semiconductor circuit board of which is formed a variable gain amplifier circuit, comprising:

a current source;

first and second MOS transistors each comprising a source connected to output of the current source;

a third MOS transistor that is connected between the source of the first MOS transistor and the source of the second MOS transistor and to a gate of which a control voltage is applied for controlling respective differential amplification gain of the first and second MOS transistors; and

a bias circuit which comprises a fourth MOS transistor comprising a source is connected to a power supply and a gate and drain are connected together and a fifth MOS transistor that is connected to the fourth MOS transistor in series and comprises a gate connected to a drain, and supplies a DC bias voltage for operating the third MOS transistor in a non-saturated region.